the changes made to the previous version of the claims, is filed herewith.

REMARKS

In view of the foregoing amendments and the following remarks, the applicants respectfully submit that the pending claims are not anticipated under 35 U.S.C. § 102. Accordingly, it is believed that this application is in condition for allowance. If, however, the Examiner believes that there are any unresolved issues, or believes that some or all of the claims are not in condition for allowance, the applicant respectfully requests that the Examiner contact the undersigned to schedule a telephone Examiner Interview before any further actions on the merits.

The applicants will now address each of the issues raised in the outstanding Office Action.

Rejections under 35 U.S.C. § 102

Claims 1-10 stand rejected under 35 U.S.C. § 102(a) as being anticipated by the current application's own purportedly admitted prior art. The applicants respectfully request that the Examiner reconsider and withdraw this ground of rejection in view of the following.

Since claim 10 has been canceled, the rejection of this claim is rendered moot.

Independent claims 1-6, as amended, are not anticipated by the purported prior art because the purported prior art does not teach a number N of gate electrode groups, where N is the minimum number corresponding to a periodic unit about connections to connection terminals within successive pixel rows, and connection terminals being combined to reduce the number of connection terminals to less than N. Each of these claims, as amended, is reprinted below with these features depicted in bold typeface:

> 1. A solid-state imaging device comprising:
>
> a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;
>
> a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;
>
> shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and
>
> a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,
>
> **the gate electrodes making up N of gate electrode groups** in which the lines belonging to each coset of modulo N within successive pixel rows are connected to common lead lines, **N** being a predetermined natural number between 4 and one half the number of pixels in a column, and **also being a minimum**

number corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, the gate electrodes having common connection terminals to reduce the number of the connection terminals to less than N. [Emphasis added.]

2. A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

gate control lines connected to gate electrode groups in which horizontal lines belonging to each coset of modulo N within successive pixel rows are connected commonly, N being a predetermined natural number between 4 and one half the number of pixels in a column, and **also being a minimum number corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, being combined with each other so**

as to reduce the number of the connection terminals to less than N. [Emphasis added.]

3. A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes being provided in a predetermined number N of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N, **N** being a predetermined natural number between 4 and one half the number of pixels in a column, and **also being a minimum number corresponding to the periodic unit about connections to said connection terminals within said successive pixel rows, some of the gate electrode groups being commonly connected so that the connection terminals are less in number than N.** [Emphasis added.]

4. A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates;

and a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes making up N of gate electrode groups in which the lines belonging to each coset of modulo N within successive pixel rows are connected to common lead lines, **N** being a predetermined natural number between 4 and one half the number of pixels in a column, and **also being a minimum number corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, the gate electrode groups having common connections to reduce the number of the connection terminals to less than N,**

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving. [Emphasis added.]

5. A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

gate control lines connected to gate electrode groups in which the horizontal lines belonging to each coset of modulo N within successive pixel rows are connected commonly, **N** being a predetermined natural number between 4 and one half the number of pixels in a column, and **also being a minimum number corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, being combined with each other so as to reduce the number of the connection terminals to less than N,**

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out

modes by selective shift gate driving. [Emphasis added.]

6. A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes being provided in a predetermined number N of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N, **N** being a predetermined natural number between 4 and one half the number of pixels in a column, and **also being a minimum number corresponding to the periodic unit about connections to said connection terminals within successive pixel rows, some of the gate electrode groups being commonly connected so that the connection terminals are less in number than N,**

wherein the commonly connected gate electrode groups are always

controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving. [Emphasis added.]

These features are addressed below.

Independent claims 1-6, as amended, are not anticipated by the purported prior art because the purported prior art does not teach a number N of gate electrode groups, where N is the minimum number corresponding to a periodic unit about connections to connection terminals within successive pixel rows, and connection terminals are combined to reduce the number of connection terminals to less than N. As the Examiner states on page 4 of Paper No. 8, in Figure 7, the number of gate electrode groups is 16 and the number of connection terminals is also 16. Thus, in Figure 7, the number of connection terminals (i.e., 16) is not less than the number of gate electrode groups (i.e., 16) as required by independent claims 1-6. Accordingly, these claims are not anticipated by the purported prior art. Since claims 7-9 depend from claims 4-6, respectively, these claims are similarly not anticipated by the purported prior art.

New claim

New independent claim 11 is supported by Figure 3 and the accompanying description. Claim 11 recites that:

> R (e.g., 32) gate electrodes are divided into S (e.g., 16) gate groups, each gate group having R/S (e.g., 2) gate electrodes,

the R (e.g., 32) gate electrodes are divided into R/S (e.g., 2) pixel groups, each having R/(R/S) (e.g., 16) consecutive, adjacent, gate electrodes,

the i^{th} gate electrode of each pixel group, where i = 1 to R/(R/S) (e.g., 16), share a common connection terminal, and

at least two gate electrodes within a given pixel group share a common connection terminal (See, e.g., 13a and 15a, 2a and 4a, etc. of Figure 3.).

The purported prior art of Figure 7 does not show this last feature. Accordingly, the applicants believe that this new claim is allowable.

Entry of Amendments

The amendments should be entered since they place the application into condition for allowance, and raise no issues other than those already discussed in the earlier amendment. The amendments were not presented earlier because the Examiner did not call the undersigned to schedule a telephone interview as requested in the earlier amendment. Accordingly, this amendment should be entered.

Conclusion

In view of the foregoing amendments and remarks, the applicant respectfully submits that the pending claims are in condition for allowance. Accordingly, the

applicants request that the Examiner pass this application to issue.

Respectfully submitted,

October 15, 2002

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CERTIFICATE OF MAILING under 37 C.F.R. 1.8(a)

I hereby certify that this correspondence is being deposited on **October 15, 2002**, with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

John C. Pokotylo

Reg. No. 36,242

SEPARATE SHEETS WITH MARKED-UP VERSION OF CLAIMS PER 37 C.F.R § 1.121(c)(1)(ii)

1. (TWICE AMENDED) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes making up N of gate electrode groups in which the lines [within successive pixel rows] belonging to each coset of modulo N within successive pixel rows are connected to common lead lines, N being a predetermined natural number between 4 and one half the number of pixels in a column, and also being a minimum number [of N] corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, the gate electrodes having common connection terminals [being combined with N gate

electrode groups] to reduce the number of the connection terminals to less than N.

2. (TWICE AMENDED) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

gate control lines connected to gate electrode groups in which horizontal lines [within successive pixel rows] belonging to each coset of modulo N within successive pixel rows are connected commonly, N being a predetermined natural number between 4 and one half the number of pixels in a column, and also being a minimum number [of N] corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, being combined with each

other so as to reduce the number of the connection terminals to less than N.

3. (TWICE AMENDED) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes being provided in a predetermined number N[, N being a predetermined natural number between 4 and one half the number of pixels in a column,] of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N, N being a predetermined natural number between 4 and one half the number of pixels in a column, and also being a minimum number corresponding to the periodic unit about connections to

said connection terminals within said successive pixel rows, some of the gate electrode groups being commonly connected so that the connection terminals are less in number than N.

4. (TWICE AMENDED) A solid-state imaging device comprising:

_____a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

_____a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

_____shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates;

_____and a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

_____the gate electrodes making up N of gate electrode groups in which the lines [within successive pixel rows] belonging to each coset of modulo N within successive pixel rows are connected to common lead lines, N being a predetermined natural number between 4 and one half the number of pixels in a column, and also being a minimum number [of N] corresponding to a periodic unit of gate electrode connections to said connection terminals within

said successive pixel rows, the gate electrode groups having common connections [electrodes being combined with N gate electrode groups] to reduce the number of the connection terminals to less than N,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.

5. (TWICE AMENDED) A solid-state imaging device comprising:

_____a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

_____a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

_____shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

_____a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

_____gate control lines connected to gate electrode groups in which the horizontal lines [within successive pixel rows] belonging to each coset of modulo N within successive pixel rows are connected commonly, N being a

predetermined natural number between 4 and one half the number of pixels in a column, and also being a minimum number [of N] corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, being combined with each other so as to reduce the number of the connection terminals to less than N,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.

6. (TWICE AMENDED) A solid-state imaging device comprising:

_____a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

_____a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

_____shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

_____a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

_____the gate electrodes being provided in a predetermined number N of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N, N being a predetermined natural number between 4 and one half the number of pixels in a column, [of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N,] and also being a minimum number corresponding to the periodic unit about connections to said connection terminals within successive pixel rows, some of the gate electrode groups being commonly connected so that the connection terminals are less in number than N,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.